REMARKS

Claims 1-29 are pending in the application.

The Examiner requires a new title that is clearly indicative of the invention to which the claims are directed.

The Examiner objects to Figures 1-4 as not including the legend Prior Art.

The Examiner allows claims 5, 7, and 22-24 if rewritten in independent form to include the base and any intervening claims. The Examiner rejects claim 1 under 35 U.S.C. § 102(e) as being anticipated by Harrison (U.S. Patent No. 6,173,432). The Examiner rejects claims 2-4, 6, 8-21, and 25-29 under 35 U.S.C. § 103(a) as being anticipated by Harrison in view of Applicant Admitted Prior Art (AAPA).

The Applicants amend claims 5, 7, and 22 and adds claim 30. Claims 1-30 remain in the application.

The Applicants add no new matter and request reconsideration.

Specification

The Applicants amend the title to obviate the Examiner's objection.

Drawings

The Applicants amend Figures 1-4 to add the legend Prior Art as indicated in the Appendix. The Applicants submit new formal drawings Figures 1-9.

Claims Allowable

The Applicants rewrite claims 5, 7, and 22 in independent form to include all the limitations of the base and any intervening claims. Claims 5, 7, and 22-24 are in condition for allowance.

Claim Rejections Under § 102 and 103

The Examiner alleges Harrison discloses all of the elements recited in independent claim 1. But the Examiner appears to misunderstand the multi-link receiving mechanism disclosed and claimed. The recited multi-link receiving mechanism receives multiple data streams from multiple transmission lines bundled together to form a multi-link channel. The recited multi-link receiving mechanism includes a first and second receivers that receive first and second data streams, respectively, substantially concurrently or *in parallel* (this is recited more explicitly in new claim 30).

Harrison, on the other hand, describes a computer system 400 that includes three packetized dynamic random access memory of SyncLink DRAMs (SLDRAMs) 10a-c. The SLDRAMs 10a-c are coupled to the processor 402 and the bus bridge 412 through a bus 404. "Although the memory devices 10a-c are coupled to the same conductors of the processor bus 404, only one memory device 10a-c at a time reads or writes data, thus avoiding bus contention on the processor bus 404." Harrison, column 9, lines 21-24. Harrison, therefore, does not address an invention as presented here where a plurality of receivers receives one of a corresponding plurality of data streams, substantially concurrent or in parallel (see Figure 2 and its attendant description). Harrison simply does not appear to be pertinent to the invention disclosed herein.

More specifically, claim 1 recites *a first receiver coupled to a first data stream and a clock signal* and *a second receiver coupled to a second data stream and said clock signal.* The Examiner alleges the first receiver is any of memory blocks 10a, 10b, or 10c shown in Harrison's Figure 5. As best understood by the Applicants, the Examiner equates the recited first and second data stream to signals CA0-9 on command bus 50 and the recited clock signal to master clock signal on bus 42. But the signals CA0-9 are not distinct first and second data streams as recited. That is, the signals CA0-9 are, at best, a single first *or* second data streams but cannot be both, particularly considering that the invention is directed to a multi-link receiving mechanism as we explained above.

Claim 1 recites ... *said first receiver delaying said clock signal by a first variable delay to derive a first reference signal, and generating a first plurality of latching control signals based upon said first reference signal to latch said first plurality of data units* and *said second receiver delaying said clock signal by a second variable delay to derive a second reference signal, and generating a second plurality of latching control signals based upon said second reference signal to latch said second plurality of data units.* Notwithstanding the Examiner's references to Harrison, it is unclear which Harrison signals the Examiner alleges disclose the recited first and second reference signals. The Examiner appears to cite sections of Harrison that describe its clock generator 210's ability to produce a sequence of clock signals each having an increased delay relative to the leading edge of the master clock. But does the Examiner allege one of the delayed clock signals is the reference signal recited? If so, then which signals are the subsequently recited plurality of latching control signals that are generated responsive to the first and second reference signals? Likewise, there appears to be no distinct, separate, second reference signal from which are generated a second plurality

of latching control signals as recited (here again pointing to Harrison's lack of applicability to the presently disclosed multi-link receiving mechanism).

Conclusion

The Applicants request reconsideration and allowance of all amended claims. Alternatively, the Applicants request the Examiner provide clarification and allow the Applicants to provide further argument. The Applicants encourage the Examiner to telephone the undersigned at (503) 222-3613 if it appears an interview would be helpful in advancing the case.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313
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